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EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/545,040	Applicant(s) COL ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- Th MAILING DATE of this communication appears on the cover she t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12 June 2003 and 26 June 2003 .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on 12 June 2003 is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-34 have been considered. Claim 21 has been amended as requested.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment A as received on 12 June 2003 and Amendment B as received on 26 June 2003.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 8-20 and 26-29 rejected under 35 U.S.C. 102(b) as being taught by Abramson et al., U.S. Patent Number 5,606,670 (herein referred to as Abramson).

5. Referring to claim 1, Abramson has taught an apparatus within a pipelined microprocessor for forwarding store instruction results to a pipeline stage for execution of a load instruction, the apparatus comprising:

a. A result forwarding cache (RFC), for storing a plurality of store instruction results (Abramson column 2, lines 36-43 and columns 4-5, lines 56-7)

b. Comparison logic, for comparing a load address of the load instruction with a plurality of store addresses associated with said plurality of store instruction results to generate an address match signal (Abramson column 2, lines 49-66)

c. Control logic, configured to receive said match signal and selectively forward one of said plurality of store instruction results from said RFC to the pipeline stage in response to-said match signal (Abramson column 2, lines 49-66)

6. Referring to claim 2, Abramson has taught the apparatus of claim 1, wherein said plurality of store instruction results comprise data to be stored from the microprocessor into a memory attached thereto (Abramson column 3, lines 53-56 and columns 4-5, lines 56-7).

7. Referring to claim 3, Abramson has taught the apparatus of claim 1, wherein said load address specifies a location of data to be loaded into the microprocessor from a memory attached thereto (Abramson column 3, line s53-56 and columns 4-5, lines 56-7).

8. Referring to claim 4, Abramson has taught the apparatus of claim 1, wherein said RFC comprises a plurality of storage elements for storing a predetermined number of instruction results (Abramson column 2, lines 36-43 and columns 4-5, lines 56-7).

9. Referring to claim 5, Abramson has taught the apparatus of claim 4, wherein said instruction results are received by said RFC from an execution unit of the microprocessor (Abramson columns 4-5, lines 56-7).

10. Referring to claim 6, Abramson has taught the apparatus of claim 4, wherein said plurality of storage elements store said predetermined number of instruction results in a first-in-first-out manner (Abramson column 5, lines 49-65 and columns 6-7, lines 59-6).

11. Referring to claim 8, Abramson has taught the apparatus of claim 1, wherein said load address and said plurality of store addresses comprise virtual addresses (Abramson column 1, lines 36-52 and column 5, lines 8-13).

12. Referring to claim 9, Abramson has taught the apparatus of claim 8, wherein said virtual addresses comprise x86 linear addresses (Abramson column 1, lines 36- 52 and column 5, lines 8-13).

13. Referring to claim 10, Abramson has taught an apparatus for forwarding storehit data within stages of a pipelined microprocessor, the apparatus comprising:

a. A result forwarding cache (RFC), configured to forward a first plurality of store instruction results (Abramson column 2, lines 63-43 and column 4-5, lines 56-7)

b. A data unit configured to forward a second plurality of store instruction results (Abramson column 2, lines 36-43; columns 4-5, lines 56-7; and column 6, lines 50-58)

c. Selection logic coupled to said RFC and said data unit, for selectively providing one of said first and second plurality of store instruction results to a stage of the microprocessor pipeline executing a load instruction (Abramson columns 2-3, lines 49-3)

14. Referring to claim 11, Abramson has taught the apparatus of claim 10, wherein said load instruction comprises a load address for specifying an address of data to be loaded into the microprocessor, wherein said selection logic is configured to forward one of said first and second plurality of store instruction results only if said load address matches one or more of a first and second plurality of store addresses corresponding to said first and second plurality of store instruction results (Abramson columns 2-3, lines 49-3 and columns 4-5, lines 56-7).

15. Referring to claim 12, Abramson has taught the apparatus of claim 11, wherein selection logic forwards said first plurality of store instruction results forwarded by said RFC- at a higher

priority than said second plurality of store instructions results forwarded by said data unit if said load address matches both one or more of said first plurality of store addresses and one or more of said second plurality of store addresses (Abramson columns 2-3, lines 49-3).

16. Referring to claim 13, Abramson has taught the apparatus of claim 11, further comprising comparison logic, coupled to said selection logic, for comparing said load address with said first and second plurality of store addresses to determine whether said load address matches one or more of said first and second plurality of store addresses (Abramson column 2, lines 49-66).

17. Referring to claim 14, Abramson has taught the apparatus of claim 11, wherein said data unit is configured to forward said second plurality of store instruction results from a plurality of store buffers of the microprocessor (columns 5-6, lines 66-6 and column 6, lines 50-58).

18. Referring to claim 15, Abramson has taught the apparatus of claim 14, wherein said plurality of store buffers is configured to store said second plurality of store instruction results while said second plurality of store instruction results are written to a memory coupled to the microprocessor (Abramson column 3, lines 53-56 and columns 4-5, lines 56-7).

19. Referring to claim 16, Abramson has taught the apparatus of claim 14, wherein said data unit is configured to forward a newest one of said second plurality of store instruction results if said load address matches more than one of said second plurality of store addresses (Abramson column 1, lines 53-61).

20. Referring to claim 17, Abramson has taught the apparatus of claim 11, wherein said RFC is configured to forward a newest one of said first plurality of store instruction results if said load address matches more than one of said first plurality of store addresses (Abramson column 1, lines 53-61).

21. Referring to claim 18, Abramson has taught an apparatus for detecting storehit conditions in a pipelined microprocessor in a hierarchical manner, the apparatus comprising:

a. First comparison logic, for comparing a load instruction load address in a first stage of the pipeline with a first plurality of store addresses of first store instruction data in a plurality of stages of the pipeline subsequent to said first pipeline stage (Abramson columns 2-3, lines 49-63)

b. Second comparison logic, for comparing said load address with a second plurality of store addresses of second store instruction data in a plurality of store buffers of the microprocessor (Abramson columns 2-3, lines 49-63)

c. Control logic, coupled to said first and second comparison logic, configured to determine which of said first and second store instruction data is newest based on said first and second comparison logic comparing (Abramson columns 2-3, lines 49-3)

22. Referring to claim 19, Abramson has taught the apparatus of claim 18, wherein said first comparison logic is configured to compare virtual addresses (Abramson column 1, lines 53-62 and column 3, lines 57-61).

23. Referring to claim 20, Abramson has taught the apparatus of claim 18, wherein said second comparison logic is configured to compare physical addresses (Abramson column 1, lines 53-62 and column 5, lines 8-13).

24. Referring to claim 26, Abramson has taught a method for forwarding storehit data in a microprocessor pipeline, the method comprising:

a. Detecting a storehit condition, wherein a load instruction in a stage of the pipeline specifies data generated by a previous store instruction, wherein said data is still present in the pipeline (Abramson columns 2-3, lines 36-3)

b. Determining whether said data is present in a result forwarding cache of the microprocessor (Abramson column 2, lines 36-43 and columns 4-5, lines 56-7)

c. Selectively forwarding said data from said result forwarding cache to said stage if said data is in said result forwarding cache (Abramson column 2, lines 36-43 and columns 4-5, lines 56-7)

d. Selectively forwarding said data from a data unit of the microprocessor to said stage if said data is not in said result forwarding cache (Abramson column 2, lines 36-43; columns 4-5, lines 56-7; and column 6, lines 33-49)

25. Referring to claim 27, Abramson has taught the method of claim 26, further comprising storing results data of each store instruction executed by an execution unit of the microprocessor in said result forwarding cache (Abramson columns 4-5, lines 56-7).

26. Referring to claim 28, Abramson has taught the method of claim 26, wherein said detecting said:

a. Storehit condition comprises comparing an address of said data specified by said load instruction with a plurality of store instruction result data addresses stored in the pipeline below said stage (Abramson column 2, lines 49-66)

b. Determining said address matches one or more of said plurality of data addresses (Abramson columns 2-3, lines 49-3)

27. Referring to claim 29, Abramson has taught the method of claim 26, wherein said determining whether said data is present in said result forwarding cache comprises:

a. Comparing an address of said data specified by said load instruction with a plurality of store instruction result data addresses stored in a predetermined number of stages of the pipeline below said stage (Abramson columns 2-3, lines 49-3)

b. Wherein said predetermined number equals a number of result entries in said result forwarding cache (Abramson columns 2-3, lines 49-3; column 4, lines 22-30; and column 6, lines 59-62)

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abramson et al., U.S. Patent Number 5,606,670 (herein referred to as Abramson) in view *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (herein referred to as *In re Rose*). Abramson has not explicitly taught wherein said predetermined number of instruction results is five. However, Abramson has taught that the number of results that are stored varies and has provided an example situation (Abramson column 5, lines 49-53 and column 4, lines 22-30). It would have been obvious to adjust the number of results stored, because the exact size of the buffer or cache does not matter. See *In re Rose*.

30. Claims 21-25 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abramson et al., U.S. Patent Number 5,606,670 (herein referred to as Abramson) in view of Patterson and Hennessy's Computer Architecture A Quantitative Approach Second Edition © 1996 (herein referred to as Hennessy).

31. Referring to claim 21, Abramson has taught an apparatus for speculatively forwarding storehit data in a microprocessor pipeline, the apparatus comprising:

a. A plurality of virtual address comparators, for comparing a load address with a plurality of virtual store addresses to generate a virtual match signal (Abramson column 1, lines 53-62; columns 2-3, lines 49-63; column 3, lines 57-61; and columns 7-8, lines 49-6)

b. A plurality of physical address comparators, for comparing a physical load address translated from said virtual load address with a plurality of physical store addresses translated from said plurality of virtual store addresses to generate a physical match signal (Abramson column 1, lines 53-62; columns 2-3, lines 49-63; column 5, lines 8-13; and columns 7-8, lines 49-6)

c. Control logic, for receiving said virtual and physical match signals, said physical match signal indicates a match between said physical load address and one of said plurality of physical store addresses but said virtual match signal indicates no match between said virtual load address and one of said plurality of virtual store addresses (Abramson column 1, lines 36-52; columns 2-3, lines 49-3; column 3, line 53 to column 4, line 10; and column 8, line 66 to column 9, line 43)

32. Abramson has not taught generating a stall signal for stalling the pipeline. Hennessy has taught generating a stall signal for stalling the pipeline (Hennessy Pages 139 and 153). It would have been obvious to a person of ordinary skill in the art to incorporate the stall of Hennessy, because it would preserve the correct execution pattern when accessing slower memory. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the stall of Hennessy in the device of Abramson to ensure correct execution patterns.

33. Referring to claim 22, Abramson has taught the apparatus of claim 21, further comprising a data unit, configured to forward correct data specified by the load address to replace previously forwarded storehit data (Abramson columns 2-3, lines 49-3). Abramson has not taught wherein said control logic is configured to deassert said stall signal after said data unit forwards said correct data. Hennessy has taught to deassert the stall signal (Hennessy Pages 139 and 153). It would have been obvious to a person of ordinary skill in the art to incorporate the deassert signal of Hennessy, because it would ensure the pipeline is not stalled longer than it needs to be stalled. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the deassert signal of Hennessy in the device of Abramson to increase speed.

34. Referring to claim 23, Abramson has taught a pipelined microprocessor for speculatively forwarding storehit data from a first pipeline stage to a second pipeline stage, wherein the storehit data is specified by a load address in the second stage, comprising:

a. Address region logic, configured to receive the load address and generate a match signal to indicate whether the load address is within one of a plurality of non-

cacheable address regions of the microprocessor address space stored therein (Abramson columns 2-3, lines 49-3)

b. Forwarding logic, for forwarding the storehit data from the first stage to the second stage during a first clock cycle (Abramson columns 2-3, lines 49-3)

c. Control logic, configured to receive said match signal

35. Abramson has not taught to assert a stall signal during a second clock cycle to stall the pipeline if the load address is within one of said plurality of non-cacheable address regions. Hennessy has taught generating a stall signal for stalling the pipeline (Hennessy Pages 139 and 153). It would have been obvious to a person of ordinary skill in the art to incorporate the stall of Hennessy, because it would preserve the correct execution pattern when slower, non-cacheable memory must be accessed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the stall of Hennessy in the device of Abramson to ensure correct execution patterns.

36. Referring to claim 24, Abramson has taught the microprocessor of claim 23, further comprising:

a. A bus interface unit, for receiving data from a bus coupled to the microprocessor, said bus further coupled to a system memory and a plurality of peripheral devices (Abramson column 1, lines 53-56 and column 4, lines 11-21)

b. At least one response buffer, operatively coupled to the second stage, for receiving load data specified by the load address from said bus interface unit, and for providing said load data to the second stage to replace the storehit data if the load address is within one of said plurality of non-cacheable address regions

(Abramson column 1, lines 53-56; column 4, lines 11-21; and column 6, lines 33-58).

37. Referring to claim 25, Abramson has taught the microprocessor of claim 23, wherein said plurality of non-cacheable regions stored in said address region logic are software-programmable (Abramson column 6, lines 33-58). In regards to Abramson, it is inherent that the non-cacheable regions are software programmable since that is how data is written and changed.

38. Referring to claim 30, Abramson has taught a method for speculatively forwarding storehit data in a microprocessor pipeline, the method comprising:

a. Speculatively forwarding storehit data from a first stage to a second stage of the pipeline based on a virtual address comparison between a load address and a plurality of store addresses (Abramson column 1, lines 18-30 and columns 2-3, lines 36-3)

b. Detecting a virtual aliasing condition with respect to said load address and one of said plurality of store addresses based on a physical address comparison between said load address and said plurality of store addresses after said speculatively forwarding (Abramson column 1, lines 53-62 and column 3, lines 57-1)

39. Abramson has not taught stalling the pipeline in response to said detecting said virtual aliasing condition. Hennessy has taught stalling the pipeline in response to said detecting said virtual aliasing condition (Hennessy Pages 139 and 153). It would have been obvious to a person of ordinary skill in the art to incorporate the stall of Hennessy, because it would preserve the correct execution pattern when accessing slower memory. Therefore, it would have been

obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the stall of Hennessy in the device of Abramson to ensure correct execution patterns.

40. Referring to claim 31, Abramson has taught the method of claim 30, further comprising forwarding correction data from a third stage of the pipeline to said second stage after said stalling the pipeline (Abramson columns 2-3, lines 49-3). Abramson has not taught unstalling the pipeline after said forwarding said correction data. Hennessy has taught unstalling the pipeline after said forwarding said correction data. (Hennessy Pages 139 and 153). It would have been obvious to a person of ordinary skill in the art to incorporate the unstall of Hennessy, because it would ensure the pipeline it not stalled longer than it needs to be stalled. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the unstall of Hennessy in the device of Abramson to increase speed.

41. Referring to claim 32, Abramson has taught the method of claim 30, wherein said virtual aliasing condition comprises a condition wherein said load address and one of said plurality of store addresses are different, but wherein said load address and said one of said plurality of store addresses map to an identical physical address (Abramson column 1, lines 36-61).

42. Referring to claim 33, Abramson has taught the method of claim 30, wherein said storehit data comprises a store instruction result within the pipeline having an identical physical store address as said physical load address (Abramson column 1, lines 36-39).

43. Referring to claim 34, Abramson has taught a method for speculatively forwarding storehit data in a microprocessor pipeline, the method comprising:

a. Detecting a storehit condition by comparing a load address with a plurality of store addresses (Abramson columns 2-3, lines 49-3)

b. Speculatively forwarding storehit data in response to said detecting said storehit condition (Abramson columns 2-3, lines 49-3 and columns 4-5, lines 56-7)

c. Determining said load address is within a non-cacheable address region subsequent to said speculatively forwarding (Abramson columns 2-3, lines 49-3 and column 6, lines 36-49)

44. Abramson has not taught stalling the pipeline in response to said determining said load address is within a non-cacheable address region. Hennessy has taught stalling the pipeline in response to said determining said load address is within a non-cacheable address region (Hennessy Pages 139 and 153). It would have been obvious to a person of ordinary skill in the art to incorporate the stall of Hennessy, because it would preserve the correct execution pattern when slower, non-cacheable memory must be accessed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the stall of Hennessy in the device of Abramson to ensure correct execution patterns.

Response to Arguments

45. Examiner withdraws the objection to the declaration in favor of the new declaration.

46. Examiner withdraws the objection to the specification in favor of the amended specification.

47. Examiner withdraws the objections to the drawings in favor of the proposed drawing corrections.

48. Examiner withdraws the 35 USC 112 second paragraph rejection to claim 21 in favor of the amended claim 21.

49. Applicant's arguments filed 26 June 2003 have been fully considered but they are not persuasive.

50. Applicant's argue on page 13 and 15 essentially that "Applicant respectfully asserts that *Abramson* does not teach an RFC." This has not been found persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the specific details of the results forwarding cache) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

51. Applicant's argue on page 14 essentially that

> "The selection logic of *Abramson* selects between one of multiple buffer slots in the store buffer to forward..., not between the store buffer and an RFC to forward store instructions results. In contrast, the selection logic as recited 10, selects between store instructions results of the data unit and the RFC."

52. This has not been found persuasive. The exact device disclosed in Abramson is an example embodiment of his device (Abramson column 12, lines 14-22), and it is possible for there to be one or more buffers present in Abramson's device (Abramson column 6, lines 50-58). When there is more than one buffer present, selection logic will select from the RFC, or its equivalent, and another store buffer.

53. Applicant's argue on page 15 essentially that

> "Applicant can find no teaching in *Abramson* of the first comparison logic recited in claim 18, which compares the load address with store addresses in a plurality of

pipeline stages other than the store buffer store addresses, which are compared by the second comparison logic..."

54. This has not been found persuasive. Abramson has taught comparing the current address with addresses in the buffer (Abramson column 2, line 49-66 and column 7, lines 49-66). Abramson has also taught multiple buffers, as mentioned above, (Abramson column 6, lines 50-58) and multiple comparators to compare buffer addresses with the current address (Abramson column 9, lines 1-7 and 21-43).

55. Applicant's argue on pages 16-17 essentially that

"...clarify the meaning of physical address as an address translated from a virtual address. Applicant can find no teaching in *Abramson* of an apparatus for speculatively forwarding storehit data having a plurality of physical address comparators...

...

...Applicant can find no teaching in *Abramson* of physical address comparators that compare a physical load address translated from a virtual load address with a plurality of physical store addresses translated from a plurality of virtual store addresses to generate a physical match signal..."

56. This has not been found persuasive. According to the definition recited by the applicant, which states that "the meaning of physical address as an address translated from a virtual address", the art still reads upon the claim. The linear addresses are compared (Abramson column 8, line 66 to column 9, line 43). The linear addresses are translated from virtual addresses (Abramson column 3, line 51 to column 4, line 10). Also, Abramson has taught

comparing physical addresses is a well-known method in the art to check for address conflicts (Abramson column 1, lines 36-61).

57. Applicant's argue on pages 17-18 essentially that "Applicant further points out that the meaning of the term 'speculative' as used by *Abramson* is different from the meaning used...". This has not been found persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the meaning of the term "speculative") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The meaning of "speculative" referred to by the application must be in the claim due to the variety of meanings for the word "speculative" found in the art and in general use.

58. Applicant's argue on pages 17 and 18 essentially that

> "Applicant can find no teaching in *Abramson* of address region logic that stores a plurality of non-cacheable regions of a microprocessor address space, and generates a match signal to indicate whether a load address is within one of the stored plurality of non-cacheable address regions."

59. This has not been found persuasive. Abramson has taught eligibility detection circuitry which takes into account memory type (Abramson column 7, lines 62-66 and column 10, line 32-49), as admitted by the applicant (page 17, paragraph 3 "*Abramson* teaches load eligibility detection circuitry having a decoder that receives a load operation's memory type and responsively outputs a signal to indicate whether the load operation's memory type is an eligible

memory type for store forwarding"), and generates signals based on these results. It is well known in the art that when referring to memory type that non-cacheable memory is included, since it is a type of memory.

60. Applicant's argue on page 18 essentially that

> "*Abramson* does not teach detecting a virtual aliasing condition with respect to a load address and one of a plurality of store addresses based on a physical address comparison between the load address and the plurality of store addresses after speculatively forwarding storehit data from a first microprocessor stage to a second microprocessor stage based on a virtual address comparison."

61. This has not been found persuasive. Abramson has taught virtual aliasing (Abramson column 1, lines 36-52; column 3, line 51 to column 4, line 10; and column 9, lines 21-43). Abramson has not explicitly called these operations virtual aliasing, however, he has taught the operational equivalent to virtual aliasing. He has disclosed that it is possible for more than one virtual address to reference the same physical and linear addresses and a detection circuit for detecting when there is an overlap of virtual addresses.

Conclusion

62. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

63. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

64. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

65. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

66. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

September 16, 2003

EDDIE CHAN
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